In the Claims

1. [currently amended] A nonvolatile EPROM or EEPROM memory cell formed using a vertical MOS transistor comprising:

a semiconductor substrate doped to have a first conductivity type so as to act as a source region of said nonvolatile memory cell, said first conductivity type being either N-type or P-type, and having a top surface which extends horizontally ~~laterally~~ and a depth which extends vertically;

a vertical MOS transistor formed by alternating, abutting N-type and P-type doped layers in said substrate which have junctions therebetween to form a channel region and a drain region of said vertical MOS transistor with said drain region having said first conductivity type and said channel region having a second conductivity type which is P-type if said first conductivity type is N-type and is N-type if said first conductivity type is P-type, said substrate forming a source region of said first conductivity type of said vertical MOS transistor, said source regions having a junction with said channel region, and wherein a well with one or more walls is etched vertically down through ~~into~~ said top surface of said substrate and through said channel and drain regions and at least partially into said source region such that at least said drain and channel regions surround said well and form at least a portion of said one or more walls of said well, said well having a bottom and having formed therein a self aligned floating gate of conductive material ~~formed therein~~ which does not have any horizontal component on said top surface of said substrate through which said well was etched nor on said bottom of said well and which does ~~is self aligned to~~ not extend laterally beyond a perimeter ~~edges~~ of said well ~~and covers all vertical surfaces of said well~~, said ~~edges~~ perimeter of said well being defined by an intersection of said one or more walls of said

well and said surface of said substrate into which said well was etched, ~~and said self~~ aligned floating gate insulated from said channel and drain regions and said substrate by a ~~self aligned~~ layer of insulating material, said floating gate being laterally adjacent to at least said portion of said wall of said well formed by said channel region of said vertical MOS transistor such that differing levels of trapped charge in said floating gate affects the conductivity of said channel region and a threshold of said nonvolatile memory cell ~~in the form of a vertical MOS transistor;~~

a word line contact which also functions as a control gate of said nonvolatile memory cell comprising a layer of conductive material formed on said substrate so as to extend vertically down into said well and lie laterally adjacent to said floating gate but be insulated therefrom by an insulation layer such that voltage applied to said control gate affects the charge on said floating gate;

a spacer insulating layer formed on top and side surfaces of said word line contact, with an edge of said spacer insulating layer defining an inner edge of a contact hole to said drain region, said inner edge being an edge of said contact hole closest to said well; and

a self aligned bit line and contact to the drain area of said vertical MOS transistor, said self aligned bit line comprising a layer of conductive material formed on said substrate so as to be in electrical contact with said drain region of said vertical MOS transistor via a self aligned contact hole.

2. [currently amended] A substructure of a vertical MOS transistor forming part of a nonvolatile memory cell comprising:

~~a semiconductor substrate having a top surface which extends in a~~ horizontal ~~lateral~~ direction and a thickness which extends in a vertical direction and having a drain region of a first conductivity type formed therein and suitable to act as a drain of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel of a vertical MOS transistor formed in said substrate;

a source region of said semiconductor substrate below said channel region, said source region being doped so as to have said first conductivity type and suitable to act as a source of a vertical MOS transistor;

a well etched vertically into said top surface of said semiconductor substrate, said well having one or more side walls and being deep enough to penetrate through said drain region and be surrounded on all sides by said drain region and said channel region and extending at least partially into said source region such that at least some portions of said one or more side walls of said well are defined by intersections with said source, drain and channel regions, said well also having a bottom;

an insulating layer covering the bottom of said well;

a gate insulating layer formed on said one or more ~~sidewalls~~ side walls of said well;

a self aligned floating gate formed in said well ~~without using any critical mask~~ comprising a conductive material formed within said well on said gate insulating layer on each wall of said well but formed so as to not have any horizontal component of

conductive material which lies on said top surface of said substrate through which said well was etched nor any horizontal component on said bottom of said well nor any conductive material which extends beyond a perimeter of said well, said perimeter defined as the intersection of said one or more walls of said well and said top surface of said substrate through which said well was etched, said self aligned floating gate ~~and~~ positioned laterally adjacent to said ~~the~~ intersection of said one or more side walls and said channel region such that trapped charge in said floating gate affects the conductivity of said channel regions and a threshold of said vertical MOS transistor~~, where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit~~;

an insulating layer formed over said self aligned floating gate so as to electrically isolate said floating gate from all surrounding structures; and

a word line comprising conductive material deposited so as to extend into said well far enough to lie laterally adjacent to said floating gate so as to form a control gate of a vertical MOS transistor nonvolatile EEPROM or EPROM memory cell structure.

3. [currently amended] A nonvolatile memory cell array comprising:

a semiconductor substrate having a top surface which extends horizontally ~~laterally~~ and having a depth which extends vertically;

an array of nonvolatile memory cells arranged ~~as a plurality of nonvolatile memory cells arranged~~ into rows and columns, said rows having a longest axis along which said nonvolatile memory cells are spaced and said columns having a longest axis along which said nonvolatile memory cells are spaced, and wherein

each nonvolatile memory cell in each row shares a common drain region with a neighboring memory cell to the left in said row and shares a common drain region with a neighboring memory cell to the right in said row, and wherein each drain region in each row is contacted by a bit line through a self aligned contact window, and wherein each memory cell in a column shares a word line which also acts as a control gate at the location of each memory cell, and wherein each said nonvolatile memory cell in said array is comprised of:

a nonvolatile EEPROM or EPROM memory cell ~~which is formed using a vertical MOS transistor (hereafter just referred to as a vertical MOS transistor or nonvolatile memory cell),~~ comprising:

a vertical MOS transistor formed by a first layer of said semiconductor substrate of N-type conductivity forming a drain region of said vertical MOS transistor, a second layer of said substrate of P-type conductivity and vertically adjacent to and beneath said first layer relative to said top surface of said substrate so as to form a channel region of said vertical MOS transistor, and a third layer of said substrate of N-type conductivity within said substrate and vertically adjacent to and beneath said second layer relative to said top surface of said substrate so as to form a source region of said vertical MOS transistor, said substrate also having a well vertically etched therein so as to penetrate through said top surface and said first and second layers and at least partially through said third layer such that said well is surrounded on all sides by said

drain region, said well having at least a portion of the wall or walls thereof formed by the intersection of said well with said drain and channel regions, and said well having a self aligned floating gate of conductive material formed therein as ~~which is self aligned by virtue of having been formed without the use of a critical mask so as to form~~ an annulus of ~~with~~ conductive material ~~of said floating gate~~ on each vertical wall of said well and formed so as to not extend horizontally ~~laterally~~ beyond the intersection of said ~~wall or~~ walls of said well and said top surface, said floating gate not having any horizontal component of conductive material on said top surface of said substrate or on a bottom surface of said well and including at least a portion thereof which lies laterally adjacent to said portion of said ~~wall or~~ walls of said well formed by the intersection of said well with said channel region such that trapped charge in said floating gate affects the conductivity of said channel regions and a threshold of said vertical MOS transistor, said floating gate being insulated from said walls of said well by a layer of gate insulating material ~~from said first, second and third layers, where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit~~;

a portion of said word line acting as a control gate of said nonvolatile memory cell, said control gate comprising a layer of

conductive material formed so as to extend down into said well and have at least a portion thereof which is laterally adjacent to said floating gate but insulated therefrom by an insulation layer so as to act as said control gate for said vertical MOS transistor;

a self aligned drain contact formed from a portion of said bit line for a row of said array in which said vertical MOS transistor is formed, said bit line comprising a layer of conductive material formed above said top surface of said substrate and passing over each said nonvolatile memory cell in said row of said array in which said nonvolatile memory cell is formed and filling self aligned drain contact windows on each side of said well in a row of which said vertical MOS transistor is a part so as to be in electrical contact with said shared drain regions of each side of said well in a row of which said vertical MOS transistor is a part; and

a spacer layer of insulating material insulating said word line from said bit line and wherein portions of said spacer layer insulating outer edges of said word line which forms a control gate of said nonvolatile memory cell define the inner edge of said self aligned drain contact window on each side of said well in a row of which said nonvolatile memory cell is a part, said inner edge of said self aligned contact windows being defined as the edges closest to said well, and wherein said outer edges of said word line are defined as edges of said word line farthest from a center of said well

along said longest axis of a row of said array of which said nonvolatile memory cell is a part.

4. [previously amended] The apparatus of claim 3 wherein said bit line is formed above said first layer so as to be above the top surface of said substrate and passes over said word lines at the location of each said nonvolatile memory cell and wherein said self aligned contact windows extend from said outer edge of each word line to the closest outer edge of an adjacent word line, where an adjacent word line is defined as a word line in an immediately adjacent column of said array, the structure of said self aligned drain contact windows thereby being such that each said bit line of a row of said array contacts each said first layer shared drain region at all points that form a top surface of said first layer between said spacer layers of insulating material that insulate said outer edges of said adjacent word lines.

5. [previously added] The apparatus of claim 3 wherein said memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said bit line contacts said first layer at at least some points between said spacer layers of the word lines of adjacent memory cells and runs over the top of word lines said bit line has to cross and is insulated from each said word line at the location of each said memory cell by said spacer layer.

6. [cancelled in response to restriction requirement]

7. [Currently amended] A vertically integrated nonvolatile memory MOS transistor formed along a long axis of a row of nonvolatile memory transistors in a memory array, comprising:

a substrate having a top surface that extends horizontally and a depth which extends vertically and which is doped to a have a first conductivity type and having an active area therein doped to a second conductivity type and a conductivity level suitable to act as a source region of a vertically integrated MOS nonvolatile memory transistor;

a buried channel region in said active area doped to have said first conductivity type and a conductivity suitable to act as a channel region of said vertically integrated MOS nonvolatile memory transistor;

a drain region in said active area doped to have said second conductivity type and a conductivity suitable to act as a drain region of said vertically integrated MOS nonvolatile memory transistor;

a well etched vertically down through said <u>top surface of said substrate and through said</u> drain and channel regions and at least partially into said source region so as to be surrounded on all sides by said drain and channel regions and so as to be on a long axis of a row of said nonvolatile memory transistors in a memory array;

~~an~~ <u>a</u> gate insulation layer formed on the walls of said well and an insulating layer on a floor of said well;

a self aligned conductive floating gate formed on all walls of said well ~~without using any critical mask~~ so as to form an annulus and formed so as to never

have any horizontal component on a bottom surface of said well and never have any horizontal component which extends onto said top surface of said substrate and outside the intersection of said walls of said well and said top surface of said substrate, said self aligned floating gate also being ~~and~~ formed on said gate insulation layer such that all portions of the walls of said well that intersect said channel region are horizontally adjacent said floating gate such that trapped charge on said floating gate can alter the conductivity of said channel region and the threshold of said vertically integrated MOS nonvolatile memory transistor~~, where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit~~;

an intergate insulation layer formed on said floating gate suitable to insulate said floating gate from all surrounding conductive structures;

a conductive control gate formed in said well so as to be horizontally adjacent to said floating gate such that a first potential applied to said control gate causes charges to tunnel into said floating gate and a second potential applied to said control gate causes charges to tunnel out of said floating gate, said control gate extending up to and making contact with or being part of a conductive word line formed across said top surface of said substrate;

a control gate insulating layer which insulates the top of said word line and one or more spacer insulation layers which insulate the sides of said word line the outer edges of said spacer insulation layer defining the inner edges of a self aligned contact hole to said drain region on each side of said well along said long

axis of said row of said nonvolatile memory transistors in an array, said outer edges being defined as the edges farthest from the center line of said well in a direction along said long axis of said row;

two self aligned contact windows which are etched so as to be self aligned to said outer edges of said spacer insulation layers and which open said drain region to electrical contact on each side of said well along said long axis of said row; and

a conductive bit line formed across said top surface of said substrate along said long axis of said row so as to make contact with said drain region through each of said two self aligned contact windows.

8. [cancelled]

9. [previously added] The apparatus of claim 1 wherein said nonvolatile memory cell is formed with a process which simultaneously forms PMOS and NMOS devices on the same substrate as said nonvolatile memory cell but forms said PMOS and NMOS devices in different active areas from an active area in which said nonvolatile memory cell is formed, and wherein said source, channel and drain regions of said nonvolatile memory cell are formed with said process which simultaneously forms said PMOS and NMOS devices and are formed while said active areas of said PMOS and NMOS devices are covered by an insulation layer.

10. [currently amended] In a vertically integrated nonvolatile memory cell structure

formed using a vertical well that penetrates down through a top surface of a substrate and into doped drain and channel regions and into a source region of ~~a~~ said substrate such that said doped drain and channel regions are adjacent to at least two sides of said well, said two sides being sides orthogonal to a long axis of a row of nonvolatile memory cells in an array of nonvolatile memory cells of which said vertically integrated nonvolatile memory cell structure is a part, said vertical well having a top edge defined by the intersection of vertical walls of said well with said ~~a~~ top surface of said substrate ~~drain region~~ and having a horizontal bottom surface, a self aligned floating gate substructure comprising:

a self aligned floating gate insulating material layer on said vertical walls of said well which does not ever extend above said top edge of said well;

an insulating layer on said bottom of said well;

a self aligned floating gate conductor material formed on said self aligned floating gate insulating material so as to form an annulus that covers all vertical walls of said well as so as to not ever any horizontal component on said bottom of said well and not ever have any horizontal component which extends above said top edge of said vertical well onto said top surface of said substrate.~~, said self aligned floating gate conductor material formed without using a critical mask, , where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit.~~

11. [previously added] The apparatus of claim 10 further comprising a self aligned layer of silicon dioxide/nitride/silicon dioxide (hereafter ONO) covering said self aligned

floating gate conductor material, and a doped polysilicon conductor control gate covering said ONO layer, said control gate extending above said top edge of said well, and a layer of silicon dioxide insulator covering a top surface of said control gate and self aligned spacer layers of silicon dioxide insulating side edges of said control gate, said ONO layer being self aligned so as to not extend horizontally beyond said side edges of said control gate.

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12. [cancelled]

13. [previously added] The apparatus of claim 10 wherein said self aligned floating gate substructure is formed by the following process:

forming a vertical well by etching vertically through a layer of silicon dioxide (herafter oxide) covering a top surface of said substrate of semiconductor material, and etching vertically down into said substrate through said doped drain and channel regions and into said source region;

depositing a layer of nitride insulator on the bottom of said well and on pad oxide formed on vertical side walls of said well and on horizontal surfaces of an insulating layer over said drain region;

anisotropically etching said nitride back from all horizontal surfaces to leave nitride only on said vertical walls of said well;

growing a layer of oxide on said bottom of said well;

wet etching said nitride off said vertical walls of said well to expose said pad oxide;

growing said self aligned floating gate insulating material layer only on said vertical walls of said well since the bottom of said well is already covered by an oxide layer and a top surface of said substrate is also already covered by an oxide layer;

depositing a layer of doped polysilicon over said substrate and into said well to cover said vertical walls and bottom of said well;

forming a self aligned floating gate without using a mask by etching back said doped polysilicon from all horizontal surfaces thereby removing all doped polysilicon from a top surface of said oxide layer which covers said top surface of said substrate and said bottom of said vertical well and leaving doped polysilicon on all vertical walls of said well.

14. [currently amended] The apparatus of claim 11 wherein said self aligned floating gate substructure, said self aligned control gate and said self aligned ONO layer are formed by the following process:

1) forming a vertical well by etching vertically through a layer of silicon dioxide (~~herafter~~ hereafter oxide) covering a top surface of said substrate of semiconductor material, and etching vertically down into said substrate through said doped drain and channel regions and into said source region;

2) depositing a layer of nitride insulator on the bottom of said well and on pad oxide formed on vertical side walls of said well and on horizontal surfaces of an insulating layer over said drain region;

3) anisotropically etching said nitride back from all horizontal surfaces to

leave nitride only on said vertical walls of said well;

4) growing a layer of oxide on said bottom of said well;

5) wet etching said nitride off said vertical walls of said well to expose said pad oxide;

6) growing said self aligned floating gate insulating material layer only on said vertical walls of said well since the bottom of said well is already covered by an oxide layer and a top surface of said substrate is also already covered by an oxide layer;

7) depositing a layer of doped polysilicon conductor over said substrate and into said well to cover said vertical walls and bottom of said well;

8) forming a self aligned floating gate ~~without using a critical mask~~ by etching back said doped polysilicon from all horizontal surfaces thereby removing all doped polysilicon from a top surface of said oxide layer which covers said top surface of said substrate and from said bottom of said vertical well and leaving doped polysilicon on all vertical walls of said well~~, where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit~~;

9) forming a layer of silicon dioxide insulator covered by a layer of nitride insulator covered by another layer of silicon dioxide insulator (hereafter ONO) over said oxide layer covering said top surface of said substrate, said ONO layer extending down into said vertical well and covering said self aligned floating gate;

10) depositing over said ONO layer a second layer of doped polysilicon conductor from which said self aligned control gate will be formed;

~~11) growing a layer of oxide over said second layer of doped polysilicon;~~

12) ~~using a non critical mask to etch~~ etching away portions of said second layer of doped polysilicon to define lateral extents of said self aligned control gate above said top surface of said substrate leaving said layer of oxide on a top surface of said control gate;

13) depositing a layer of oxide over said surface of said substrate and covering said control gate's vertical side walls;

14) anisotropically etching back said layer of oxide deposited in step 13 to remove oxide only from horizontal surfaces and leaving spacer oxide only on vertical side walls of said polysilicon of said control gate and word line thereby defining outer edges of said spacer oxide layer where said outer edges are edges of said spacer oxide layer which are farthest from a centerline of said well in a direction along said long axis of said row;

15) ~~using a non critical mask~~ photolithographically etching to define the lateral extents of contact holes to said drain region etching through said ONO layer formed in step 9 and said oxide layer covering said top surface of said substrate to self align said ONO layer to the lateral extents of said control gate and leave two contact holes to said drain regions adjacent to said two side of said well which are orthogonal to said long axis of said row of nonvolatile memory cells in said array of nonvolatile memory cells, said contact holes being self aligned to said outer edges of said spacer oxide layer.

15. [currently amended] In a vertically integrated nonvolatile memory cell structure

~~formed using a vertical well that penetrates~~ a top surface of a semiconductor substrate into doped drain and channel regions of said substrate and into a source region of ~~a~~ said substrate, said vertical well having a top edge and a bottom, a self aligned floating gate insulating layer substructure comprising:

a self aligned floating gate insulating material layer on all vertical walls of said well and formed in such a way that said self aligned floating gate insulating material ~~which~~ does not extend above the top of said well; and

an insulating layer on the bottom of said well.

16. [cancelled]